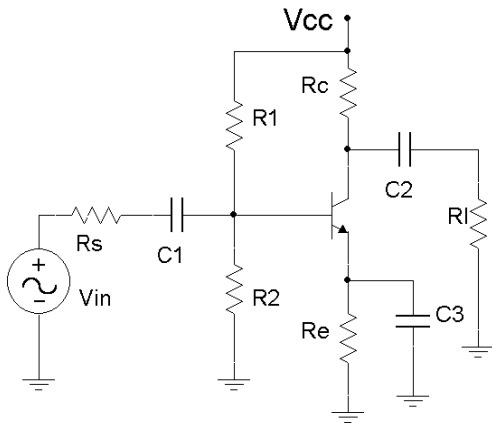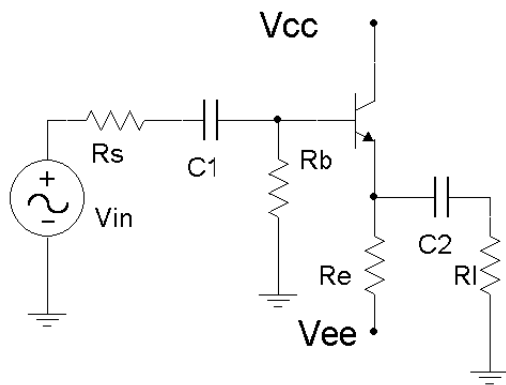# Class A Power Amplifier Worksheet

ET161 Linear Electronics, Prof. Fiore

For the circuits below determine the output compliance, maximum load power, efficiency and worst case transistor ratings (P_D, BV_{CEO}, I_{C-MAX}). Assume $\beta=200$ and Rs=0.

For circuit one, Vcc=30V, R1=2k, R2=1k, Re=465, Rc=600, Rload=400.

For circuit two, Vcc=15V, Vee=-20V, Re=100, Rb=400, Rload=50.

The solutions are on the following pages.

Circuit One Solutions

DC Analysis: Assuming unloaded divider, V_B=30V*1k/(1k+2k)=10VDC. Therefore, V_E=9.3VDC and I_E=9.3V/465=20mA. $I_{CQ}{\approx}I_E$.
V_{Rc}=20mA*600=12VDC and therefore V_C=30V-12V=18VDC.
Finally, V_{CEQ}=V_C-V_E=18V-9.3V=8.7VDC.

The transistor's average power dissipation, P_D, is the quiescent power, or I_{CQ}*V_{CEQ}.
P_D=20mA*8.7V=174mW

Total circuit power is the total voltage supplied times the total current. The total current equals the collector current (20mA) plus the divider current (assuming unloaded divider, 30V/3k=10mA), or 30mA.
P_{DC}=30V*30mA=900mW

AC Analysis: The load line endpoints are
$I_{C(sat)}$=I_{CQ}+V_{CEQ}/(r_C+r_E)
$I_{C(sat)}$=20mA+8.7/(400||600+0)
$I_{C(sat)}$=20mA+8.7/240
$I_{C(sat)}$=20mA+36.25mA=56.25mA
This represents the worst case transistor current, $I_{C\text{-}MAX}$

$V_{CE(cutoff)}$=V_{CEQ}+I_{CQ}(r_C+r_E)
$V_{CE(cutoff)}$=8.7+20mA(400||600+0)
$V_{CE(cutoff)}$=8.7+20mA*240
$V_{CE(cutoff)}$=8.7+4.8=13.5V
This represents the worst case transistor voltage, BV_{CEO}

The compliance is the smaller swing, i.e., 8.7V vs. 4.8V, so the compliance is 4.8V peak (9.6Vpp or 3.39Vrms). Therefore, the maximum load power is
$P_{L\text{-}max}$=rms compliance^2/r_L
$P_{L\text{-}max}$=3.39^2/400=28.8mW

η= $P_{L\text{-}max}$/P_{DC}
η= 28.8mW/900mW=3.2%

This is a low power but then again the load is rather high at 400 ohms.

Circuit Two Solutions

DC Analysis: Assuming $V_B \approx 0V$, $V_E = -.7VDC$ and $I_E = 19.3V/100 = 193mA$. $I_{CQ} \approx I_E$. $V_C = V_{CC} = 15VDC$ and therefore $V_{CEQ} = V_C - V_E = 15V - (-.7V) = 15.7VDC$.

The transistor's average power dissipation, P_D, is the quiescent power, or $I_{CQ} * V_{CEQ}$. $P_D = 193mA * 15.7V = 3.03W$

Total circuit power is the total voltage supplied times the total current. The total current equals the collector current (193mA) while the total voltage is $15V - (-20V) = 35V$. $P_{DC} = 35V * 193mA = 6.755W$

AC Analysis: The load line endpoints are
$I_{C(sat)} = I_{CQ} + V_{CEQ}/(r_C + r_E)$
$I_{C(sat)} = 193mA + 15.7/(0 + 100\|50)$
$I_{C(sat)} = 193mA + 15.7/33.3$
$I_{C(sat)} = 193mA + 471mA = 664mA$
This represents the worst case transistor current, $I_{C\text{-}MAX}$

$V_{CE(cutoff)} = V_{CEQ} + I_{CQ}(r_C + r_E)$
$V_{CE(cutoff)} = 15.7 + 193mA(0 + 100\|50)$
$V_{CE(cutoff)} = 15.7 + 193mA * 33.3$
$V_{CE(cutoff)} = 15.7 + 6.4 = 22.1V$
This represents the worst case transistor voltage, BV_{CEO}

The compliance is the smaller swing, i.e., 15.7V vs. 6.4V, so the compliance is 6.4V peak (12.8Vpp or 4.52Vrms). Therefore, the maximum load power is
$P_{L\text{-}max} = \text{rms compliance}^2/r_L$
$P_{L\text{-}max} = 4.52^2/50 = 409mW$

$\eta = P_{L\text{-}max}/P_{DC}$
$\eta = 409mW/6.755W = 6.06\%$

50 Ohms would be typical for headphones or earbuds and 409mW would be loud under normal conditions. Both circuits produce cutoff clipping before saturation clipping but this is not always the case. Also, better circuits would exhibit a centered Q point causing saturation and cutoff clipping to occur simultaneously. This produces the best efficiency.